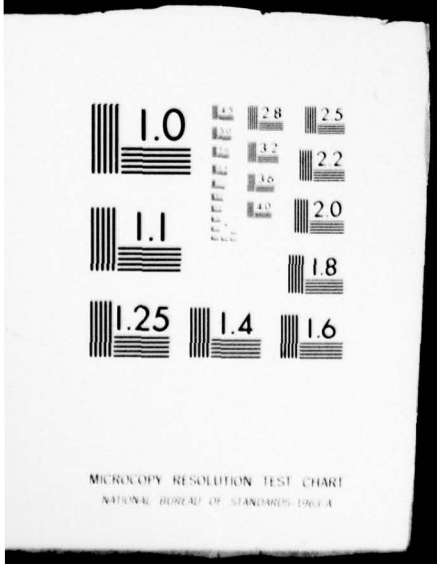
AD-A071 740 CORNELL UNIV ITHACA N Y SCHOOL OF ELECTRICAL ENGINEERING F/G 20/12
THE USE OF AL(X)GA(1-X)AS BUFFER LAYERS TO REDUCE PARASITIC SPA--ETC(U)
JUN 79 L F EASTMAN, D W WOODWARD, A CHANDRA N00014-75-C-0739
UNCLASSIFIED NL

| OF |
AD A071740

END
DATE FILMED
8-79
DDC

OF 1

071740



(15) N00014-75-

(6) The Use of
Space Charg
in FET Str

(10) By Z
Les

A sim

space char
or buffer.
agreement
obtained
fabricated
The paras
strate or
domain th
Including
drain bia
as the sq
root of t

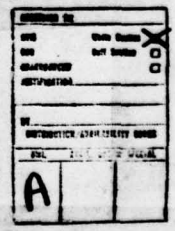
GaAs

Al_xGa_{1-x}

junction
reduced
devices

AD A071740

DDC FILE COPY



N0014-75-C-0739 LEVEL II

79

The Use of $Al_xGa_{1-x}As$ Buffer Layers to Reduce Parasitic Space Charge Limited Current Flow Through the Substrate in FET Structures

By L.F. Eastman, D.W. Woodard, A. Chandra and M. Shur

A simple analysis has been made of the parasitic space charge limited current flow in a GaAs substrate or buffer. The computed output conductance is in agreement with experimental values of 600 to 1000 ohms obtained on low noise FET's with 300 μm gate width fabricated on GaAs buffer layers with low trap density. The parasitic current flows in the semi-insulating substrate or buffer layer, around the thin high field Gunn domain that is present in the active layer of the FET. Including the effects of changing domain length with drain bias, the parasitic current is found to rise as the square root of the drain voltage and as the 4th root of the active channel doping.

GaAs FET's were fabricated with undoped high purity $Al_xGa_{1-x}As$ buffer layers in order to utilize the heterojunction barrier and reduced saturation velocity to provide reduced parasitic conduction. Output conductance of these devices are in the range of 5000 ohms.